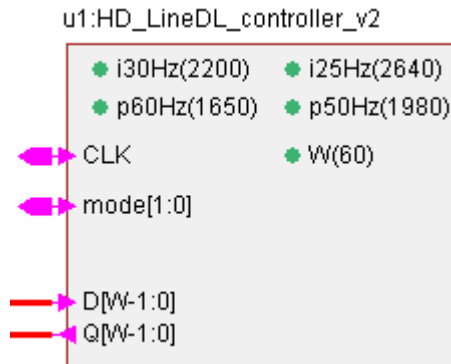




- Delay time: one video frame line;
- Video format: 1080i/30, 1080i/25, 720p/60, 720p/50
- Video data stream clock: 74.25MHz
- Destination platform: Xilinx FPGA Virtex II, Spartan 3, Altera Cyclone, etc.

(see module source code in APPENDIX A)

## Description



### Ports:

**CLK** –pixel data clock input;  
**mode[1:0]** –video format input: “0”- 720p/50, “1”- 720p/60, “2”- 1080i/25, “3”- 1080i/30;  
**D[W-1:0]** –input data bus, where W is a bus width;  
**Q[W-1:0]** –output data bus, where W is a bus width;

### Parameters (Fig.1):

**i30Hz** –number of pixels in picture line for 1080i/30 mode. Usually equals to 2200;  
**i25Hz** –number of pixels in picture line for 1080i/25 mode. Usually equals to 2640;  
**p60Hz** –number of pixels in picture line for 720p/60 mode. Usually equals to 1650;  
**p50Hz** –number of pixels in picture line for 720p/50 mode. Usually equals to 1980;  
**W** –number of bits of input and output buses.

**APPENDIX A**

```

module HD_LineDL_controller_v2 (CLK, D, Q, mode) ;
parameter
    i30Hz = 2200 ,      //1080i,30
    i25Hz = 2640 ,      //1080i,25
    W = 16 ,
    p60Hz = 1650 ,      //720p,60
    p50Hz = 1980 ;      //720p,50

input          CLK;
input          [W-1:0] D;
output        [W-1:0] Q;
input         [1:0] mode;

reg           [W-1:0] RAM [4095:0]
    /* syn_ramstyle="no_rw_check" */ /* synthesis syn_ramstyle="block_ram" */;

reg [11:0] w_addr, r_addr ;
reg [11:0] Tdelay;

always @*
    case (mode)
        2'd0:      Tdelay[11:0] = p50Hz;
        2'd1:      Tdelay[11:0] = p60Hz;
        2'd2:      Tdelay[11:0] = i25Hz;
        2'd3:      Tdelay[11:0] = i30Hz;
        default:   Tdelay[11:0] = i30Hz;
    endcase

always @(posedge CLK) r_addr[11:0] = r_addr[11:0] + 12'd1;
always @(negedge CLK) w_addr[11:0] <= r_addr[11:0] + Tdelay;
always @(posedge CLK) RAM[w_addr] <= D;

//always @(RAM or r_addr) Q = RAM[r_addr];
assign Q = RAM[r_addr];

endmodule //HD_LineDL_controller_v2(a0)

```